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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,718	12/08/2003	Donald C. Stark	9797-0147-999	5477

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,718	STARK ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/8/03&9/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 30-79 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-29 of U.S. Patent No. 6163178. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent claims and the application claims recite the same scope.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 49-79 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 49 and 64 are indefinite because there is no antecedent basis for the limitation "the circuit".

Claims 50-63 and 65-79 are rejected as including the indefiniteness of claim 49 or 64.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 49-51, 54 and 56-58 are rejected under 35 U.S.C. 102(b) as being anticipated by Taylor et al. (USP 5182467).

As to claim 49, Taylor et al. discloses in figure 3 an integrated circuit device comprising a multiplexor (14) to select data (odd-data and even-data) in response to a clock signal (BUFCLOCK2), wherein a data bit of the data is selected in response to a transition of the clock signal; a predriver (16), coupled to the circuit, to adjust a slew rate of the data signal (circuit 16 is a buffer that shaping or adjusting the slew rate the output data signal MUXOUT); a voltage generator (circuit, not shown, that generating voltage VDD) coupled to the predriver, to generate a supply voltage VDD for the prior driver; and an output driver (18) coupled to the predriver, the output driver including a plurality of transistor stacks (figure 7 shows that circuit 18 comprises plurality of transistor stacks Q37, Q41 and Q38, Q42) to adjust an output drive level of the output driver.

As to claim 50, figure 3 show that the drive level of the output driver is programmable to adjust the output drive level in accordance with a value that is representative of a drive level.

As to claim 51, figure 7 shows a subset of the plurality of transistor stacks, i.e. Q38 and Q42, are selected to adjust the output drive level of the output driver, wherein the output drive level is based on a predetermined amount of current.

As to claim 54, figure 7 shows that a transistor, i.e. Q41 and Q42, in each transistor stack of the plurality of transistor stacks has an associated predetermined threshold voltage (it is inherent that transistor has threshold), and an output voltage from the predriver has a maximum value corresponding to the predetermined threshold voltage such that the transistor operates in saturation when outputting a predetermined low-level output voltage (when transistor Q41 or Q42 is ON, operating in saturation, it output a low level).

As to claim 56, figure 6 shows that the predriver (16) includes a base block (Q28, Q29, D13-D16, C4, C5, Q31, Q32) and at least one slew rate adjustment block (L1, L2, R5-R8, Q21, Q22, Q25-Q27) coupled in parallel with the base block, the at least one slew rate adjustment block responsive to a slew rate control signal (ONE/ZERO CONTROL).

As to claim 57, circuit, not shown, that generating the ONE/ZERO CONTROL signal is seen as the claimed "circuit for increasing a rate at which an output from the predriver transitions from a high-level supply voltage to a low-level supply voltage (the not shown circuit controls the slew rate of the output of the predrive, wherein the slew rate can be increased or decreased).

As to claim 58, figure 7 shows that an output impedance of each transistor stack is maintained within a predetermined range (any value may be considered as predetermined range) when the transistor stack is outputting a low voltage level.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 55 are 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. (USP 5182467).

As to claim 55, Taylor et al.'s figure 3 fails to teach that the predetermined threshold voltage is substantially between 0.3 and 0.4 Volts. However, the selection of the thresold voltage of the transistor to be between 0.3 and 0.4 volts is seen as an obvious design preference dependent upon particular environment of use to ensure optimum performance.

As to claim 59, Taylor et al.'s figure 3 fails to teach that the output impedance is substantially exceeds 150 ohms. However, the selection for the output impedance to be exceed 150 ohms is seen as an obvious design preference dependent upon particular environment of use to ensure optimum performance.

9. Claims 64-66 and 69-75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al. (USP 5182467) in view of Sugibayashi (USP 5373477).

Taylor et al.'s figure 3 shows all limitations of the claims except for "a charge compensation circuit to provide an amount of charge to a supply voltage for the predriver in accordance with a charge compensation value". However, it is notoriously well known in the art that voltage regulator is used for providing a stable supply voltage. Sugibayashi's figure 5 shows a voltage regulator providing a stable supply voltage independent of the external supply voltage. Therefore, it would have been obvious to one having ordinary skill in the art to use Sugibayashi's voltage regulator for generating voltage VDD in Taylor et al.'s figure 3 in order to improving the circuit performance. Thus, the modified Taylor et al.'s figure 3 further shows a charge compensation circuit (Sugibayashi's 12e, 12f) to provide an amount of charge to a supply voltage for the predriver in accordance with a charge compensation value.

Allowable Subject Matter

10. Claims 30-48 would be allowable if Applicant submitted a terminal disclaimer to over come the Double Patenting rejection above.

11. Claims 52, 53, 60-63, 67, 68 and 76-78 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 30-48 would be allowable because the prior art fails to teach or suggest a circuit, coupled to the multiplexor, to regulate a duty cycle of a data signal corresponding to the data in accordance with the clock signal.

Claims 52 and 67 would be allowable because the prior art fails to teach or suggest each that transistor stack of the plurality of transistor stacks is binary weighted with respect a transistor in another transistor stack of the plurality of transistor stacks.

Claims 53 and 68 would be allowable because the prior art fails to teach or suggest that transistors in the plurality of transistor stacks are sized such that a current drive capability of the output driver is binary weighted.

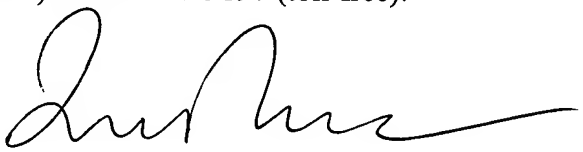
Claims 60-63 and 76-78 would be allowable because the prior art fails to teach or suggest a charge compensation value generator, coupled to the charge compensation circuit, the charge compensation value generator including a voltage generator, a test circuit; and a logic circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Quan Tra
Patent Examiner

October 12, 2004